Design For Manufacturability And Yield For Nano Scale Cmos

Yield and Variability Optimization of Integrated CircuitsIntegrated Product Design and Manufacturing Using Geometric Dimensioning and TolerancingIEEE/SEMI International Semiconductor Manufacturing Science SymposiumSystem-on-Chip Test ArchitecturesDesign and Process Integration for Microelectronic ManufacturingIntegrated Circuit and System DesignCost Reduction and Optimization for Manufacturing and Industrial CompaniesSemiconductorsManufacturing Yield Evaluation of VLSI/WSI SystemsEncyclopedia of MicrocomputersSix Sigma for Electronics Design and ManufacturingNano-CMOS Design for ManufacturabilityNano-CMOS Circuit and Physical DesignIntegrated Circuit ManufacturabilityFrom Contamination to Defects, Faults and Yield LossDefect-Oriented Testing for Nano-Metric CMOS VLSI CircuitsSemiconductorsDesign for Manufacturability and Statistical DesignMicroelectronic Manufacturing Yield, Reliability, and Failure AnalysisNanoscale CMOS VLSI Circuits: Design for ManufacturabilityDesign for Manufacturability and Statistical DesignVLSI Design for Manufacturing: Yield EnhancementIstc/cstic 2009 (cistc)Electronic Design Automation for IC Implementation, Circuit Design, and Process TechnologyDesign for Manufacturability and Yield for Nano-Scale CMOSMicroelectronics Manufacturability, Yield, and ReliabilityProcess Variations in Microsystems ManufacturingDesign of Fault-tolerant Programmable Logic Arrays for Yield

EnhancementDesign for ManufacturabilityDesign for ManufacturingDesign for Manufacturing (DFM) in Submicron VLSI DesignMaterials Enabled DesignsVLSI Design for Manufacturing: Yield EnhancementArtificial Neural Networks – ICANN 2009Process Variations and Probabilistic Integrated Circuit DesignDesign for Manufacturability Through Design-process IntegrationAnalog Design Centering and SizingDesign for Manufacturability of Ceramic ComponentsEDA for IC Implementation, Circuit Design, and Process TechnologyStrain-Engineered MOSFETs

Yield and Variability Optimization of Integrated Circuits

This volume is part of the two-volume proceedings of the 19th International Conf- ence on Artificial Neural Networks (ICANN 2009), which was held in Cyprus during September 14–17, 2009. The ICANN conference is an annual meeting sp- sored by the European Neural Network Society (ENNS), in cooperation with the - ternational Neural Network Society (INNS) and the Japanese Neural Network Society (JNNS). ICANN 2009 was technically sponsored by the IEEE Computational Intel- gence Society. This series of conferences has been held annually since 1991 in various European countries and covers the field of neurocomputing, learning systems and related areas. Artificial neural networks provide an information-processing structure inspired by biological nervous systems. They consist of a large number of highly interconnected processing elements, with the

capability of learning by example. The field of artificial neural networks has evolved significantly in the last two decades, with active partici- tion from diverse fields, such as engineering, computer science, mathematics, artificial intelligence, system theory, biology, operations research, and neuroscience. Artificial neural networks have been widely applied for pattern recognition, control, optimization, image processing, classification, signal processing, etc.

Integrated Product Design and Manufacturing Using Geometric Dimensioning and Tolerancing

A practical understanding of these concepts and their application can help to reduce the chance of having device failures.

IEEE/SEMI International Semiconductor Manufacturing Science Symposium

This book constitutes the refereed proceedings of the 14th International Workshop on Power and Timing Optimization and Simulation, PATMOS 2004, held in Santorini, Greece in September 2004. The 85 revised papers presented together with abstracts of 6 invited presentations were carefully reviewed and selected from 152 papers submitted. The papers are organized in topical sections on buses and communication, circuits and devices, low power issues, architectures, asynchronous circuits, systems design, interconnect and physical design, security and safety, low-power processing, digital design, and modeling and

simulation.

System-on-Chip Test Architectures

Focuses on rapid implementation of practical, real-world cost reduction solutions In today's economic climate, the need to cut costs can be the difference between success and failure. Cost Reduction and Optimization for Manufacturing and Industrial Companies covers all major cost reduction areas, providing easy to read examples and advice on steps to take. It provides the roadmap for implementing recommended actions with true and tried methods by taking a modern, all-inclusive look at manufacturing processes. Based on the author's cost reduction experience gained during 30 years of senior operations and consulting engagements with hundreds of organizations, this book includes easy-to-understand and easy-to-implement cost reduction concepts organized into five general areas --labor, material, design, process, and overhead. Each chapter: Dives into a cost reduction area and starts with the bottom line first by summarizing key points Provides proven tactics for cutting costs without a lot of extraneous data Follows a qualitative and design-oriented approach Emphasizes quick implementation and measurable cost reduction Identifies who in the organization should do the work Outlines risks and suggested risk mitigation actions Contains numerous tables, graphs, and photos to show the concepts described in the book Praise for Cost Reduction and Optimization for Manufacturing and Industrial Companies "In this introductory book, Berk not only

takes a modern, all-inclusive look at manufacturing processes but also provides substantial coverage of engineering materials and production systems. It follows a more qualitative and design-oriented approach than other texts in the market, helping readers gain a better understanding of important concepts. They'll also discover how micro-economic conditions relate to the process variables in a given process as well as how to perform manufacturing science and quantitative engineering analysis of manufacturing processes." —Fred Silverman, Director Engineering of Hi-Shear Technology Corporation "Joe Berk has created a unique, practical and straightforward approach to cost reduction in manufacturing. This work provides valuable insights and concrete techniques, based on real-world experiences, to any manufacturing organization undertaking change to position itself to compete successfully in the global marketplace." —Joe Carleone, President and COO of American Pacific Corporation Check out author Joseph Berk's blog at http://manufacturingtraining.wordpress.com/

Design and Process Integration for Microelectronic Manufacturing

Visual Fidelity: Designing Multimedia Interfaces for Active Learning to Xerox Corporation

Integrated Circuit and System Design

Cost Reduction and Optimization for

Manufacturing and Industrial Companies

ISTC/CSTIC is an annual semiconductor technology conference covering all the aspects of semiconductor technology and manufacturing, including devices, design, lithography, integration, materials, processes, manufacturing as well as emerging semiconductor technologies and silicon material applications. ISTC/CSTIC 2009 was merged by ISTC (International Semiconductor Technology Conference) and CSTIC (China Semiconductor Technology International Conference), the two industry leading technical conferences in China, and consisted of one plenary session and nine technical symposia. This issue of ECS Transactions contains 159 papers from the conference.

Semiconductors

Cutting-Edge CMOS VLSI Design for Manufacturability Techniques This detailed guide offers proven methods for optimizing circuit designs to increase the yield, reliability, and manufacturability of products and mitigate defects and failure. Covering the latest devices, technologies, and processes, Nanoscale CMOS VLSI Circuits: Design for Manufacturability focuses on delivering higher performance and lower power consumption. Costs, constraints, and computational efficiencies are also discussed in the practical resource. Nanoscale CMOS VLSI Circuits covers: Current trends in CMOS VLSI design Semiconductor manufacturing technologies Photolithography Process and device variability:

analyses and modeling Manufacturing-Aware Physical Design Closure Metrology, manufacturing defects, and defect extraction Defect impact modeling and yield improvement techniques Physical design and reliability DFM tools and methodologies

Manufacturing Yield Evaluation of VLSI/WSI Systems

Encyclopedia of Microcomputers

As VLSI technology scales to 65nm and below, traditional communication between design and manufacturing becomes more and more inadequate. Gone are the days when designers simply pass the design GDSII Ơ1le to the foundry and expect very good man℗Ơufacturing and parametric yield. This is largely due to the enormous challenges in the manufacturing stage as the feature size continues to shrink. Thus, the idea of DFM (Design for Manufacturing) is getting very popular. Even though there is no universally accepted deƠ1nition of DFM, in my opinion, one of the major parts of DFM is to bring manufacturing information into the design stage in a way that is understood by designers. Consequently, designers can act on the information to improve both manufacturing and parametric yield. In this dissertation, I will present several attempts to reduce the gap between design and manufacturing communities: Alt-PSM aware standard cell designs, printability improve℗Ơment for detailed routing and the ASIC design Ơ2ow with litho aware static timing

analysis. Experiment results show that we can greatly improve the manufacturability of the designs and we can reduce design pessimism signiƟ1cantly for easier design closure.

Six Sigma for Electronics Design and Manufacturing

Because of the continuous evolution of integrated circuit manufacturing (ICM) and design for manufacturability (DfM), most books on the subject are obsolete before they even go to press. That's why the field requires a reference that takes the focus off of numbers and concentrates more on larger economic concepts than on technical details. Semiconductors: Integrated Circuit Design for Manufacturability covers the gradual evolution of integrated circuit design (ICD) as a basis to propose strategies for improving return-on-investment (ROI) for ICD in manufacturing. Where most books put the spotlight on detailed engineering enhancements and their implications for device functionality, in contrast, this one offers, among other things, crucial, valuable historical background and roadmapping, all illustrated with examples. Presents actual test cases that illustrate product challenges, examine possible solution strategies, and demonstrate how to select and implement the right one This book shows that DfM is a powerful generic engineering concept with potential extending beyond its usual application in automated layout enhancements centered on proximity correction and pattern density. This material explores the concept of ICD for production by

breaking down its major steps: product definition, design, layout, and manufacturing. Averting extended discussion of technology, techniques, or specific device dimensions, the author also avoids the clumsy chapter architecture that can hinder other books on this subject. The result is an extremely functional, systematic presentation that simplifies existing approaches to DfM, outlining a clear set of criteria to help readers assess reliability, functionality, and yield. With careful consideration of the economic and technical trade-offs involved in ICD for manufacturing, this reference addresses techniques for physical, electrical, and logical design, keeping coverage fresh and concise for the designers, manufacturers, and researchers defining product architecture and research programs.

Nano-CMOS Design for Manufacturability

This book explains integrated circuit design for manufacturability (DfM) at the product level (packaging, applications) and applies engineering DfM principles to the latest standards of product development at 22 nm technology nodes. It is a valuable guide for layout designers, packaging engineers and quality engineers, covering DfM development from 1D to 4D, involving IC design flow setup, best practices, links to manufacturing and product definition, for process technologies down to 22 nm node, and product families including memories, logic, system-on-chip and system-in-package.

Nano-CMOS Circuit and Physical Design

There are books aplenty on materials selection criteria for engineering design. Most cover the physical and mechanical properties of specific materials, but few offer much in the way of total product design criteria. This innovative new text/reference will give the “Big picture view of how materials should be selected—not only for a desired function but also for their ultimate performance, durability, maintenance, replacement costs, and so on. Even such factors as how a material behaves when packaged, shipped, and stored will be taken into consideration. For without that knowledge, a design engineer is often in the dark as to how a particular material used in particular product or process is going to behave over time, how costly it will be, and, ultimately, how successful it will be at doing what is supposed to do. This book delivers that knowledge. * Brief but comprehensive review of major materials functional groups (mechanical, electrical, thermal, chemical) by major material categories (metals, polymers, ceramics, composites) * Invaluable guidance on selection criteria at early design stage, including such factors as functionality, durability, and availability * Insight into lifecycle factors that affect choice of materials beyond simple performance specs, including manufacturability, machinability, shelf life, packaging, and even shipping characteristics * Unique help on writing materials selection specifications

Integrated Circuit Manufacturability

Papers from the symposium deal with concepts, applications, and grinding and machining aspects in ceramic component design for manufacturability (DFM). Topics include probabalistic DFM, processing technology for advanced structural ceramics, rapid prototyping applied to industrial design of ceramics

From Contamination to Defects, Faults and Yield Loss

Currently strain engineering is the main technique used to enhance the performance of advanced silicon-based metal-oxide-semiconductor field-effect transistors (MOSFETs). Written from an engineering application standpoint, Strain-Engineered MOSFETs introduces promising strain techniques to fabricate strain-engineered MOSFETs and to methods to assess the applications of these techniques. The book provides the background and physical insight needed to understand new and future developments in the modeling and design of n- and p-MOSFETs at nanoscale. This book focuses on recent developments in strain-engineered MOSFETS implemented in high-mobility substrates such as, Ge, SiGe, strained-Si, ultrathin germanium-on-insulator platforms, combined with high-k insulators and metal-gate. It covers the materials aspects, principles, and design of advanced devices, fabrication, and applications. It also presents a full technology computer aided design (TCAD) methodology for strain-engineering in Si-CMOS technology involving data flow from process simulation to process variability simulation via device simulation and generation of SPICE process compact

models for manufacturing for yield optimization. Microelectronics fabrication is facing serious challenges due to the introduction of new materials in manufacturing and fundamental limitations of nanoscale devices that result in increasing unpredictability in the characteristics of the devices. The down scaling of CMOS technologies has brought about the increased variability of key parameters affecting the performance of integrated circuits. This book provides a single text that combines coverage of the strain-engineered MOSFETS and their modeling using TCAD, making it a tool for process technology development and the design of strain-engineered MOSFETs.

Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits

Design for Manufacturability and Statistical Design: A Comprehensive Approach presents a comprehensive overview of methods that need to be mastered in understanding state-of-the-art design for manufacturability and statistical design methodologies. Broadly, design for manufacturability is a set of techniques that attempt to fix the systematic sources of variability, such as those due to photolithography and CMP. Statistical design, on the other hand, deals with the random sources of variability. Both paradigms operate within a common framework, and their joint comprehensive treatment is one of the objectives of this book and an important differentation.

Semiconductors

This book addresses the preparation and application of design layout analyses with concurrent engineering teams in six steps that capture design intent and add value to design process. It offers tools for eliminating costly trial-and-error approaches and deliver economically viable products. The authors discuss product design techniques that allevi

Design for Manufacturability and Statistical Design

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DfM is a powerful generic engineering concept with potential extending beyond its usual application in automated layout enhancements centered on proximity correction and pattern density. This material explores the concept of ICD for production by breaking down its major steps: product definition, design, layout, and manufacturing. Averting extended discussion of technology, techniques, or specific device dimensions, the author also avoids the clumsy chapter architecture that can hinder other books on this subject. The result is an extremely functional, systematic presentation that simplifies existing approaches to DfM, outlining a clear set of criteria to help readers assess reliability, functionality, and yield. With careful consideration of the economic and technical trade-offs involved in ICD for manufacturing, this reference addresses techniques for physical, electrical, and logical design, keeping coverage fresh and concise for the designers, manufacturers, and researchers defining product architecture and research programs.

Microelectronic Manufacturing Yield, Reliability, and Failure Analysis

Design for Manufacturing assists anyone not familiar with various manufacturing processes in better visualizing and understanding the relationship between part design and the ease or difficulty of producing the part. Decisions made during the early conceptual stages of design have a great effect on subsequent stages. In fact, quite often more than 70% of the manufacturing cost of a product is

determined at this conceptual stage, yet manufacturing is not involved. Through this book, designers will gain insight that will allow them to assess the impact of their proposed design on manufacturing difficulty. The vast majority of components found in commercial batch-manufactured products, such as appliances, computers and office automation equipment are either injection molded, stamped, die cast, or (occasionally) forged. This book emphasizes these particular, most commonly implemented processes. In addition to chapters on these processes, the book touches upon material process selection, general guidelines for determining whether several components should be combined into a single component or not, communications, the physical and mechanical properties of materials, tolerances, and inspection and quality control. In developing the DFM methods presented in this book, he has worked with over 30 firms specializing in injection molding, die-casting, forging and stamping. Implements a philosophy which allows for easier and more economic production of designs Educates designers about manufacturing Emphasizes the four major manufacturing processes

Nanoscale CMOS VLSI Circuits: Design for Manufacturability

Over the years there has been a large increase in the functionality available on a single integrated circuit. This has been mainly achieved by a continuous drive towards smaller feature sizes, larger dies, and better packing efficiency. However, this greater functionality

has also resulted in substantial increases in the capital investment needed to build fabrication facilities. Given such a high level of investment, it is critical for IC manufacturers to reduce manufacturing costs and get a better return on their investment. The most obvious method of reducing the manufacturing cost per die is to improve manufacturing yield. Modern VLSI research and engineering (which includes design manufacturing and testing) encompasses a very broad range of disciplines such as chemistry, physics, material science, circuit design, mathematics and computer science. Due to this diversity, the VLSI arena has become fractured into a number of separate sub-domains with little or no interaction between them. This is the case with the relationships between testing and manufacturing. From Contamination to Defects, Faults and Yield Loss: Simulation and Applications focuses on the core of the interface between manufacturing and testing, i.e., the contamination-defect-fault relationship. The understanding of this relationship can lead to better solutions of many manufacturing and testing problems. Failure mechanism models are developed and presented which can be used to accurately estimate probability of different failures for a given IC. This information is critical in solving key yield-related applications such as failure analysis, fault modeling and design manufacturing.

Design for Manufacturability and Statistical Design

Traditionally, Computer Aided Design (CAD) tools

have been used to create the nominal design of an integrated circuit (IC), such that the circuit nominal response meets the desired performance specifications. In reality, however, due to the disturbances ofthe IC manufacturing process, the actual performancesof the mass produced chips are different than those for the nominal design. Even if the manufacturing process were tightly controlled, so that there were little variations across the chips manufactured, the environmentalchanges (e. g. those oftemperature, supply voltages, etc.) would alsomakethe circuit performances vary during the circuit life span. Process-related performance variations may lead to low manufacturing yield, and unacceptable product quality. For these reasons, statistical circuit design techniques are required to design the circuit parameters, taking the statistical process variations into account. This book deals with some theoretical and practical aspects of IC statistical design, and emphasizes how they differ from those for discrete circuits. It de scribes a spectrum of different statistical design problems, such as parametric yield optimization, generalized on-target design, variability minimization, per formance tunning, and worst-case design. The main emphasis of the presen tation is placed on the principles and practical solutions for performance vari ability minimization. It is hoped that the book may serve as an introductory reference material for various groups of IC designers, and the methodologies described will help them enhance the circuit quality and manufacturability. The book containsseven chapters.

VLSI Design for Manufacturing: Yield Enhancement

Proceedings of SPIE present the original research papers presented at SPIE conferences and other high-quality conferences in the broad-ranging fields of optics and photonics. These books provide prompt access to the latest innovations in research and technology in their respective fields. Proceedings of SPIE are among the most cited references in patent literature.

Istc/cstic 2009 (cistc)

This book thoroughly examines and explains the basic processing steps used in MEMS fabrication (both integrated circuit and specialized micro machining processing steps. The book places an emphasis on the process variations in the device dimensions resulting from these commonly used processing steps. This will be followed by coverage of commonly used metrology methods, process integration and variations in material properties, device parameter variations, quality assurance and control methods, and design methods for handling process variations. A detailed analysis of future methods for improved microsystems manufacturing is also included. This book is a valuable resource for practitioners, researchers and engineers working in the field as well as students at either the undergraduate or graduate level.

Electronic Design Automation for IC

Implementation, Circuit Design, and Process Technology

The second of two volumes in the Electronic Design Automation for Integrated Circuits Handbook, Second Edition, Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology thoroughly examines real-time logic (RTL) to GDSII (a file format used to transfer data of semiconductor physical layout) design flow, analog/mixed signal design, physical verification, and technology computer-aided design (TCAD). Chapters contributed by leading experts authoritatively discuss design for manufacturability (DFM) at the nanoscale, power supply network design and analysis, design modeling, and much more. New to This Edition: Major updates appearing in the initial phases of the design flow, where the level of abstraction keeps rising to support more functionality with lower non-recurring engineering (NRE) costs Significant revisions reflected in the final phases of the design flow, where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting-edge applications and approaches realized in the decade since publication of the previous edition—these are illustrated by new chapters on 3D circuit integration and clock design Offering improved depth and modernity, Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology provides a valuable, state-of-the-art reference for electronic design automation (EDA) students, researchers, and professionals.

Design for Manufacturability and Yield for Nano-Scale CMOS

One of the keys to success in the IC industry is getting a new product to market in a timely fashion and being able to produce that product with sufficient yield to be profitable. There are two ways to increase yield: by improving the control of the manufacturing process and by designing the process and the circuits in such a way as to minimize the effect of the inherent variations of the process on performance. The latter is typically referred to as "design for manufacture" or "statistical design". As device sizes continue to shrink, the effects of the inherent fluctuations in the IC fabrication process will have an even more obvious effect on circuit performance. And design for manufacture will increase in importance. We have been working in the area of statistically based computer aided design for more than 13 years. During the last decade we have been working with each other, and individually with our students, to develop methods and CAD tools that can be used to improve yield during the design and manufacturing phases of IC realization. This effort has resulted in a large number of publications that have appeared in a variety of journals and conference proceedings. Thus our motivation in writing this book is to put, in one place, a description of our approach to IC yield enhancement. While the work that is contained in this book has appeared in the open literature, we have attempted to use a consistent notation throughout this book.

Microelectronics Manufacturability, Yield, and Reliability

Based on the authors' expansive collection of notes taken over the years, Nano-CMOS Circuit and Physical Design bridges the gap between physical and circuit design and fabrication processing, manufacturability, and yield. This innovative book covers: process technology, including sub-wavelength optical lithography; impact of process scaling on circuit and physical implementation and low power with leaky transistors; and DFM, yield, and the impact of physical implementation.

Process Variations in Microsystems Manufacturing

Discover innovative tools that pave the way from circuit and physical design to fabrication processing Nano-CMOS Design for Manufacturability examines the challenges that design engineers face in the nano-scaled era, such as exacerbated effects and the proven design for manufacturability (DFM) methodology in the midst of increasing variability and design process interactions. In addition to discussing the difficulties brought on by the continued dimensional scaling in conformance with Moore's law, the authors also tackle complex issues in the design process to overcome the difficulties, including the use of a functional first silicon to support a predictable product ramp. Moreover, they introduce several emerging concepts, including stress proximity effects, contour-based extraction, and design process

interactions. This book is the sequel to Nano-CMOS Circuit and Physical Design, taking design to technology nodes beyond 65nm geometries. It is divided into three parts: Part One, Newly Exacerbated Effects, introduces the newly exacerbated effects that require designers' attention, beginning with a discussion of the lithography aspects of DFM, followed by the impact of layout on transistor performance Part Two, Design Solutions, examines how to mitigate the impact of process effects, discussing the methodology needed to make sub-wavelength patterning technology work in manufacturing, as well as design solutions to deal with signal, power integrity, WELL, stress proximity effects, and process variability Part Three, The Road to DFM, describes new tools needed to support DFM efforts, including an auto-correction tool capable of fixing the layout of cells with multiple optimization goals, followed by a look ahead into the future of DFM Throughout the book, real-world examples simplify complex concepts, helping readers see how they can successfully handle projects on Nano-CMOS nodes. It provides a bridge that allows engineers to go from physical and circuit design to fabrication processing and, in short, make designs that are not only functional, but that also meet power and performance goals within the design schedule.

Design of Fault-tolerant Programmable Logic Arrays for Yield Enhancement

Six Sigma is a customer-based manufacturing approach to realizing fewer defects and thus lowering

costs and increasing customer satisfaction. This is a rigorous engineering book detailing the gritty, statistical work involved in making the Six Sigma process work in the electronics industry.

Design for Manufacturability

Design for Manufacturability and Statistical Design: A Comprehensive Approach presents a comprehensive overview of methods that need to be mastered in understanding state-of-the-art design for manufacturability and statistical design methodologies. Broadly, design for manufacturability is a set of techniques that attempt to fix the systematic sources of variability, such as those due to photolithography and CMP. Statistical design, on the other hand, deals with the random sources of variability. Both paradigms operate within a common framework, and their joint comprehensive treatment is one of the objectives of this book and an important differentation.

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Design for Manufacturing (DFM) in Submicron VLSI Design

Materials Enabled Designs

VLSI Design for Manufacturing: Yield Enhancement

What you'll find here is a fascinating compendium of fundamental problem formulations of analog design

centering and sizing. This essential work provides a differentiated knowledge about the tasks of analog design centering and sizing. In particular, worst-case scenarios are formulated and analyzed. This work is right at the crossing point between process and design technology, and is both reference work and textbook for understanding CAD methods in analog sizing.

Artificial Neural Networks – ICANN 2009

Process Variations and Probabilistic Integrated Circuit Design

The 2nd edition of defect oriented testing has been extensively updated. New chapters on Functional, Parametric Defect Models and Inductive fault Analysis and Yield Engineering have been added to provide a link between defect sources and yield. The chapter on RAM testing has been updated with focus on parametric and SRAM stability testing. Similarly, newer material has been incorporated in digital fault modeling and analog testing chapters. The strength of Defect Oriented Testing for nano-Metric CMOS VLSIs lies in its industrial relevance.

Design for Manufacturability Through Design-process Integration

This book walks the reader through all the aspects of manufacturability and yield in a nano-CMOS process. It covers all CAD/CAE aspects of a SOC design flow

and addresses a new topic (DFM/DFY) critical at 90 nm and beyond. This book is a must read book the serious practicing IC designer and an excellent primer for any graduate student intent on having a career in IC design or in EDA tool development.

Analog Design Centering and Sizing

Uncertainty in key parameters within a chip and between different chips in the deep sub micron area plays a more and more important role. As a result, manufacturing process spreads need to be considered during the design process. Quantitative methodology is needed to ensure faultless functionality, despite existing process variations within given bounds, during product development. This book presents the technological, physical, and mathematical fundamentals for a design paradigm shift, from a deterministic process to a probability-orientated design process for microelectronic circuits. Readers will learn to evaluate the different sources of variations in the design flow in order to establish different design variants, while applying appropriate methods and tools to evaluate and optimize their design.

Design for Manufacturability of Ceramic Components

This book addresses the study of process and design variables to determine the ease and feasibility of fabrication -- or manufacturability -- of contemporary VLSI systems and circuits. The reader will be

introduced to the key aspects in today's design practices: yield management, defect and fault modeling, testing, and fault tolerant architectures. These four sections present the reader with practical issues normally applied in industry and usually required by quality, product, and design engineering departments. "Integrated Circuit Manufacturability" thoroughly examines the entire manufacturing process from circuit to silicon. Copyright © Libri GmbH. All rights reserved.

EDA for IC Implementation, Circuit Design, and Process Technology

Modern electronics testing has a legacy of more than 40 years. The introduction of new technologies, especially nanometer technologies with 90nm or smaller geometry, has allowed the semiconductor industry to keep pace with the increased performance-capacity demands from consumers. As a result, semiconductor test costs have been growing steadily and typically amount to 40% of today's overall product cost. This book is a comprehensive guide to new VLSI Testing and Design-for-Testability techniques that will allow students, researchers, DFT practitioners, and VLSI designers to master quickly System-on-Chip Test architectures, for test debug and diagnosis of digital, memory, and analog/mixed-signal designs. Emphasizes VLSI Test principles and Design for Testability architectures, with numerous illustrations/examples. Most up-to-date coverage available, including Fault Tolerance, Low-Power Testing, Defect and Error Tolerance, Network-on-Chip

(NOC) Testing, Software-Based Self-Testing, FPGA Testing, MEMS Testing, and System-In-Package (SIP) Testing, which are not yet available in any testing book. Covers the entire spectrum of VLSI testing and DFT architectures, from digital and analog, to memory circuits, and fault diagnosis and self-repair from digital to memory circuits. Discusses future nanotechnology test trends and challenges facing the nanometer design era; promising nanotechnology test techniques, including Quantum-Dots, Cellular Automata, Carbon-Nanotubes, and Hybrid Semiconductor/Nanowire/Molecular Computing. Practical problems at the end of each chapter for students.

Strain-Engineered MOSFETs

Presenting a comprehensive overview of the design automation algorithms, tools, and methodologies used to design integrated circuits, the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes. The second volume, EDA for IC Implementation, Circuit Design, and Process Technology, thoroughly examines real-time logic to GDSII (a file format used to transfer data of semiconductor physical layout), analog/mixed signal design, physical verification, and technology CAD (TCAD). Chapters contributed by leading experts authoritatively discuss design for manufacturability at the nanoscale, power supply network design and analysis, design modeling, and much more. Save on the complete set.

ROMANCE ACTION & ADVENTURE MYSTERY & THRILLER BIOGRAPHIES & HISTORY CHILDREN'S YOUNG ADULT FANTASY HISTORICAL FICTION HORROR LITERARY FICTION NON-FICTION SCIENCE FICTION