Design Methodology For Rf Cmos Phase Locked Loops

Parasitic-Aware Optimization of CMOS RF CircuitsRF CMOS Class C Power Amplifiers for Wireless CommunicationsLow Power RF Circuit Design in Standard CMOS TechnologyCMOS Multichannel Single-Chip Receivers for Multi-Gigabit Optical Data CommunicationsDissertation Abstracts InternationalDesign of CMOS RF Integrated Circuits and SystemsTechnical Digest 2005ProceedingsCharacterization and Optimization of the RF Performances of Analog Components in CMOS and BiCMOs TechnologiesMicrowave JournalLNA-ESD Co-Design for Fully Integrated CMOS Wireless ReceiversDistributed Computing, Artificial Intelligence, Bioinformatics, Soft Computing, and Ambient Assisted LivingRF CMOS Oscillators for Modern Wireless ApplicationsWireless Technologies: Concepts, Methodologies, Tools and ApplicationsIstc/cstic 2009 (cistc)Proceedings of the International Symposium on the Physical & Failure Analysis of Integrated CircuitsRF Power Amplifiers for Mobile CommunicationsAutomated Hierarchical Synthesis of Radio Frequency Integrated Circuits and SystemsAnalysis and Design of Quadrature OscillatorsThe Design of Low-power Integrated Radio-frequency Front-end in CMOSElectrical Overstress (EOS)Design and Modeling of Millimeter-wave CMOS Circuits for Wireless TransceiversESD Protection Device and Circuit Design for Advanced CMOS TechnologiesDevice Modeling for Analog and RF CMOS Circuit DesignMillimeter Wave Technology in Wireless PAN, LAN, and MANRF CMOS Power Amplifiers: Theory, Design and ImplementationESDDesign Methodology for RF CMOS Phase Locked LoopsCMOS RF Modeling, Characterization and ApplicationsAnalysis and Design of RF CMOS AttenuatorsVLSI-SoC: Forward-Looking Trends in IC and Systems DesignHigh Data Rate Transmitter CircuitsProceedings of the ACM Great Lakes Symposium on VLSI.Wireless Radio-Frequency Standards and System Design: Advanced TechniquesNano-scale CMOS Analog CircuitsThe Design of CMOS Radio-Frequency Integrated CircuitsAsia Electronics IndustryThe gm/ID Methodology, a sizing tool for low-voltage analog CMOS CircuitsUltra-Low Power Wireless Technologies for Sensor NetworksDesign of CMOS Phase-Locked Loops

Parasitic-Aware Optimization of CMOS RF Circuits

ISTC/CSTIC is an annual semiconductor technology conference covering all the aspects of semiconductor technology and manufacturing, including devices, design, lithography, integration, materials, processes, manufacturing as well as emerging semiconductor technologies and silicon material applications. ISTC/CSTIC 2009 was merged by ISTC (International Semiconductor Technology Conference) and CSTIC (China Semiconductor Technology International Conference), the two industry leading technical conferences in China, and consisted of one plenary session and nine technical symposia. This issue of ECS Transactions contains 159 papers from the conference.

RF CMOS Class C Power Amplifiers for Wireless Communications

Radio-frequency (RF) integrated circuits in CMOS technology are gaining increasing

popularity in the commercial world, and CMOS technology has become the dominant technology for applications such as GPS receivers, GSM cellular transceivers, wireless LAN, and wireless short-range personal area networks based on IEEE 802.15.1 (Bluetooth) or IEEE 802.15.4 (ZigBee) standards. Furthermore, the increasing interest in wireless technologies and the widespread of wireless communications has prompted an ever increasing demand for radio frequency transceivers. Wireless Radio-Frequency Standards and System Design: Advanced Techniques provides perspectives on radio-frequency circuit and systems design, covering recent topics and developments in the RF area. Exploring topics such as LNA linearization, behavioral modeling and co-simulation of analog and mixed-signal complex blocks for RF applications, integrated passive devices for RF-ICs and baseband design techniques and wireless standards, this is a comprehensive reference for students as well as practicing professionals.

Low Power RF Circuit Design in Standard CMOS Technology

RF CMOS Power Amplifiers: Theory Design and Implementation focuses on the design procedure and the testing issues of CMOS RF power amplifiers. This is the first monograph addressing RF CMOS power amplifier design for emerging wireless standards. The focus on power amplifiers for short is distance wireless personal and local area networks (PAN and LAN), however the design techniques are also applicable to emerging wide area networks (WAN) infrastructure using micro or pico cell networks. The book discusses CMOS power amplifier design principles and theory and describes the architectures and tardeoffs in designing linear and nonlinear power amplifiers. It then details design examples of RF CMOS power amplifiers for short distance wireless applications (e, g., Bluetooth, WLAN) including designs for multi-standard platforms. Design aspects of RF circuits in deep submicron CMOS are also discussed. RF CMOS Power Amplifiers: Theory Design and Implementation serves as a reference for RF IC design engineers and RD and R&D managers in industry, and for graduate students conducting research in wireless semiconductor IC design in general and with CMOS technology in particular.

CMOS Multichannel Single-Chip Receivers for Multi-Gigabit Optical Data Communications

This book describes a new design methodology that allows optimization-based synthesis of RF systems in a hierarchical multilevel approach, in which the system is designed in a bottom-up fashion, from the device level up to the (sub)system level. At each level of the design hierarchy, the authors discuss methods that increase the design robustness and increase the accuracy and efficiency of the simulations. The methodology described enables circuit sizing and layout in a complete and automated integrated manner, achieving optimized designs in significantly less time than with traditional approaches. Describes an efficient and accurate methodology to design automatically RF systems, with guaranteed accuracy from the device to the system level; Discusses analytical and machine learning techniques for modelling integrated inductors and uses such models in synthesis approaches; Compares synthesis strategies for RF circuits based on bottom-up versus flat approaches; Discusses layout-aware bottom-up design

methodologies for RF circuits; Discusses variability-aware bottom-up design methodologies for RF circuits; Describes multilevel bottom-up design methodologies from the device up to the system level.

Dissertation Abstracts International

Driven by the demand for high-data-rate, millimeter wave technologies with broad bandwidth are being explored in high-speed wireless communications. These technologies include gigabit wireless personal area networks (WPAN), high-speed wireless local area networks (WLAN), and high-speed wireless metropolitan area networks (WMAN). As a result of this technological push, standard organizations are actively calling for specifications of millimeter wave applications in the above wireless systems. Providing the guidance needed to help you navigate through these new technologies, Millimeter Wave Technology in Wireless PAN, LAN, and MAN covers the fundamental concepts, recent advances, and potential that these millimeter wave technologies will offer with respect to circuits design, system architecture, protocol development, and standardization activities. The book presents essential challenges and solutions related to topics that include millimeter wave monolithic integrated circuit (MMIC), packaging technology of millimeter wave system and circuits, and millimeter wave channel models. With numerous figures, tables and references, this text allows speedy access to the fundamental problems, key challenges, open issues, future directions, and further readings on millimeter wave technologies in relation to WPAN, WLAN, and WMAN.

Design of CMOS RF Integrated Circuits and Systems

Technical Digest 2005

Modern RF receivers and transmitters require quadrature oscillators with accurate quadrature and low phase-noise. Existing literature is dedicated mainly to single oscillators, and is strongly biased towards LC oscillators. This book is devoted to quadrature oscillatorsand presents adetailed comparative study ofLC and RCosc-lators, both at architectural and at circuit levels. It is shown that in cross-coupled RC oscillators both the quadrature error and phase-noise are reduced, whereas in LC - cillators the coupling decreases the quadrature error, but increases the phase-noise. Thus, quadrature RC oscillators can be a practical alternative to LC oscillators, - pecially when area and cost are to be minimized. The main topics of the book are: cross-coupled LC quasi-sinusoidal oscillators, cross-coupled RC relaxation oscillators, a quadrature RC oscillator-mixer, and t- integrator oscillators. The effect of mismatches on the phase-error and the pha- noise are thoroughly investigated. The book includes many experimental results, obtained from different integrated circuit prototypes, in the GHz range. A structured design approach is followed: a technology independent study, with ideal blocks, is performed initially, and then the circuit level design is addressed. This book can be used in advanced courses on RF circuit design. In addition to post-graduate students and lecturers, this book will be of interest to design engineers and researchers in this area.

Proceedings

Design and Modeling of Millimeter-wave CMOS Circuits for Wireless Transceivers describes in detail some of the interesting developments in CMOS millimetre-wave circuit design. This includes the re-emergence of the slow-wave technique used on passive devices, the license-free 60GHz band circuit blocks and a 76GHz voltage-controlled oscillator suitable for vehicular radar applications. All circuit solutions described are suitable for digital CMOS technology. Digital CMOS technology developments driven by Moore's law make it an inevitable solution for low cost and high volume products in the marketplace. Explosion of the consumer wireless applications further makes this subject a hot topic of the day. The book begins with a brief history of millimetre-wave research and how the silicon transistor is born. Originally meant for different purposes, the two technologies converged and found its way into advanced chip designs. The second part of the book describes the most important passive devices used in millimetre-wave CMOS circuits. Part three uses these passive devices and builds circuit blocks for the wireless transceiver. The book completes with a comprehensive list of references for further readings. Design and Modeling of Millimeter-wave CMOS Circuits for Wireless Transceivers is useful to show the analogue IC designer the issues involved in making the leap to millimetre-wave circuit designs. The graduate student and researcher can also use it as a starting point to understand the subject or proceed to innovative from the works described herein.

Characterization and Optimization of the RF Performances of Analog Components in CMOS and BiCMOs Technologies

IC designers appraise currently MOS transistor geometries and currents to compromise objectives like gain-bandwidth, slew-rate, dynamic range, noise, non-linear distortion, etc. Making optimal choices is a difficult task. How to minimize for instance the power consumption of an operational amplifier without too much penalty regarding area while keeping the gain-bandwidth unaffected in the same time? Moderate inversion yields high gains, but the concomitant area increase adds parasitics that restrict bandwidth. Which methodology to use in order to come across the best compromise(s)? Is synthesis a mixture of design experience combined with cut and tries or is it a constrained multivariate optimization problem, or a mixture? Optimization algorithms are attractive from a system perspective of course, but what about low-voltage low-power circuits, requiring a more physical approach? The connections amid transistor physics and circuits are intricate and their interactions not always easy to describe in terms of existing software packages. The gm/ID synthesis methodology is adapted to CMOS analog circuits for the transconductance over drain current ratio combines most of the ingredients needed in order to determine transistors sizes and DC currents.

Microwave Journal

In the arena of Parasitic-Aware Design of CMOS RF Circuits, efforts are aimed at the realization of true single-chip radios with few, if any, off-chip components. Ironically, the on-chip passive components required for RF integration pose miore serious challenges to SOC integration than the active CMOS and BJT devices. This is not surprising since modern digital IC designs are dominated as much, or more, by interconnectg characteristics than by active device properties. In any event, the

co-integration of active and passive devices in RFIC design represents a serious design problem and an even more daunting manufacturing challenge. If conventional mixed-signal design techniques are employed, parasitics associated with passive elements (resistors, capacitors, inductors, transformers, pads, etc.) and the package effectively de-tune RF circuits rendering them sub-optimal or virtually useless. Hence, dealing with parasitics in an effective way as part of the design process is an essential emerging methodology in modern SOC design. The parasitic-aware RF circuit synthesis techinques described in this book effectively address this critical problem.

LNA-ESD Co-Design for Fully Integrated CMOS Wireless Receivers

Distributed Computing, Artificial Intelligence, Bioinformatics, Soft Computing, and Ambient Assisted Living

After a review of PLL essentials, this uniquely comprehensive workbench guide takes you step-by-step through operation principles, design procedures, phase noise analysis, layout considerations, and CMOS realizations for each PLL building block. You get full details on LC tank oscillators including modeling and optimization techniques, followed by design options for CMOS frequency dividers covering flip-flop implementation, the divider by 2 component, and other key factors. The book includes design alternatives for phase detectors that feature methods to minimize jitter caused by the dead zone effect. You also find a sample design of a fully integrated PLL for WLAN applications that demonstrates every step and detail right down to the circuit schematics and layout diagrams. Supported by over 150 diagrams and photos, this one-stop toolkit helps you produce superior PLL designs faster, and deliver more effective solutions for low-cost integrated circuits in all RF applications.

RF CMOS Oscillators for Modern Wireless Applications

Wireless Technologies: Concepts, Methodologies, Tools and Applications

Istc/cstic 2009 (cistc)

Proceedings of the International Symposium on the Physical & Failure Analysis of Integrated Circuits

Reliability concerns and the limitations of process technology can sometimes restrict the innovation process involved in designing nano-scale analog circuits. The success of nano-scale analog circuit design requires repeat experimentation, correct analysis of the device physics, process technology, and adequate use of

the knowledge database. Starting with the basics, Nano-Scale CMOS Analog Circuits: Models and CAD Techniques for High-Level Design introduces the essential fundamental concepts for designing analog circuits with optimal performances. This book explains the links between the physics and technology of scaled MOS transistors and the design and simulation of nano-scale analog circuits. It also explores the development of structured computer-aided design (CAD) techniques for architecture-level and circuit-level design of analog circuits. The book outlines the general trends of technology scaling with respect to device geometry, process parameters, and supply voltage. It describes models and optimization techniques, as well as the compact modeling of scaled MOS transistors for VLSI circuit simulation. • Includes two learning-based methods: the artificial neural network (ANN) and the least-squares support vector machine (LS-SVM) method • Provides case studies demonstrating the practical use of these two methods • Explores circuit sizing and specification translation tasks • Introduces the particle swarm optimization technique and provides examples of sizing analog circuits • Discusses the advanced effects of scaled MOS transistors like narrow width effects, and vertical and lateral channel engineering Nano-Scale CMOS Analog Circuits: Models and CAD Techniques for High-Level Design describes the models and CAD techniques, explores the physics of MOS transistors, and considers the design challenges involving statistical variations of process technology parameters and reliability constraints related to circuit design.

RF Power Amplifiers for Mobile Communications

ESD Protection Device and Circuit Design for Advanced CMOS Technologies is intended for practicing engineers working in the areas of circuit design, VLSI reliability and testing domains. As the problems associated with ESD failures and yield losses become significant in the modern semiconductor industry, the demand for graduates with a basic knowledge of ESD is also increasing. Today, there is a significant demand to educate the circuits design and reliability teams on ESD issues. This book makes an attempt to address the ESD design and implementation in a systematic manner. A design procedure involving device simulators as well as circuit simulator is employed to optimize device and circuit parameters for optimal ESD as well as circuit performance. This methodology, described in ESD Protection Device and Circuit Design for Advanced CMOS Technologies has resulted in several successful ESD circuit design with excellent silicon results and demonstrates its strengths.

Automated Hierarchical Synthesis of Radio Frequency Integrated Circuits and Systems

Analysis and Design of Quadrature Oscillators

The Design of Low-power Integrated Radio-frequency Front-end in CMOS

This book constitutes the refereed proceedings of the 10th International Work-

Conference on Artificial Neural Networks, IWANN 2009, held in Salamanca, Spain in June 2009. The 167 revised full papers presented together with 3 invited lectures were carefully reviewed and selected from over 230 submissions. The papers are organized in thematic sections on theoretical foundations and models; learning and adaptation; self-organizing networks, methods and applications; fuzzy systems; evolutionary computation and genetic algoritms; pattern recognition; formal languages in linguistics; agents and multi-agent on intelligent systems; brain-computer interfaces (bci); multiobjetive optimization; robotics; bioinformatics; biomedical applications; ambient assisted living (aal) and ambient intelligence (ai); other applications.

Electrical Overstress (EOS)

LNA-ESD Co-Design for Fully Integrated CMOS Wireless Receivers fits in the quest for complete CMOS integration of wireless receiver front-ends. With a combined discussion of both RF and ESD performance, it tackles one of the final obstacles on the road to CMOS integration. The book is conceived as a design guide for those actively involved in the design of CMOS wireless receivers. The book starts with a comprehensive introduction to the performance requirements of low-noise amplifiers in wireless receivers. Several popular topologies are explained and compared with respect to future technology and frequency scaling. The ESD requirements are introduced and related to the state-of-the-art protection devices and circuits. LNA-ESD Co-Design for Fully Integrated CMOS Wireless Receivers provides an extensive theoretical treatment of the performance of CMOS low-noise amplifiers in the presence of ESD-protection circuitry. The influence of the ESD-protection parasitics on noise figure, gain, linearity, and matching are investigated. Several RF-ESD co-design solutions are discussed allowing both high RF-performance and good ESD-immunity for frequencies up to and beyond 5 GHz. Special attention is also paid to the layout of both active and passive components. LNA-ESD Co-Design for Fully Integrated CMOS Wireless Receivers offers the reader intuitive insight in the LNA’s behavior, as well as the necessary mathematical background to optimize its performance. All material is experimentally verified with several CMOS implementations, among which a fully integrated GPS receiver front-end. The book is essential reading for RF design engineers and researchers in the field and is also suitable as a text book for an advanced course on the subject.

Design and Modeling of Millimeter-wave CMOS Circuits for Wireless Transceivers

While mobile phones enjoy the largest production volume ever of any consumer electronics products, the demands they place on radio-frequency (RF) transceivers are particularly aggressive, especially on integration with digital processors, low area, low power consumption, while being robust against process-voltage-temperature variations. Since mobile terminals inherently operate on batteries, their power budget is severely constrained. To keep up with the ever increasing data-rate, an ever-decreasing power per bit is required to maintain the battery lifetime. The RF oscillator is the second most power-hungry block of a wireless radio (after power amplifiers). Consequently, any power reduction in an RF oscillator will greatly benefit the overall power efficiency of the cellular transceiver.

Moreover, the RF oscillators' purity limits the transceiver performance. The oscillator's phase noise results in power leakage into adjacent channels in a transmit mode and reciprocal mixing in a receive mode. On the other hand, the multi-standard and multi-band transceivers that are now trending demand wide tuning range oscillators. However, broadening the oscillator's tuning range is usually at the expense of die area (cost) or phase noise. The main goal of this book is to bring forth the exciting and innovative RF oscillator structures that demonstrate better phase noise performance, lower cost, and higher power efficiency than currently achievable. Technical topics discussed in RF CMOS Oscillators for Modern Wireless Applicationsinclude: Design and analysis of low phase-noise class-F oscillators Analyze a technique to reduce 1/f noise up-conversion in the oscillators Design and analysis of low power/low voltage oscillators Wide tuning range oscillators Reliability study of RF oscillators in nanoscale CMOS

ESD Protection Device and Circuit Design for Advanced CMOS Technologies

Low Power Consumption is one of the critical issues in the performance of small battery-powered handheld devices. Mobile terminals feature an ever increasing number of wireless communication alternatives including GPS, Bluetooth, GSM, 3G, WiFi or DVB-H. Considering that the total power available for each terminal is limited by the relatively slow increase in battery performance expected in the near future, the need for efficient circuits is now critical. This book presents the basic techniques available to design low power RF CMOS analogue circuits. It gives circuit designers a complete guide of alternatives to optimize power consumption and explains the application of these rules in the most common RF building blocks: LNA, mixers and PLLs. It is set out using practical examples and offers a unique perspective as it targets designers working within the standard CMOS process and all the limitations inherent in these technologies.

Device Modeling for Analog and RF CMOS Circuit Design

Millimeter Wave Technology in Wireless PAN, LAN, and MAN

This book tackles both high efficiency and high linearity power amplifier (PA) design in low-voltage CMOS. With its emphasis on theory, design and implementation, the book offers a guide for those actively involved in the design of fully integrated CMOS wireless transceivers. Offering mathematical background, as well as intuitive insight, the book is essential reading for RF design engineers and researchers and is also suitable as a text book.

RF CMOS Power Amplifiers: Theory, Design and Implementation

Contains the latest research, case studies, theories, and methodologies within the field of wireless technologies.

ESD

Design Methodology for RF CMOS Phase Locked Loops

This practical guide and introduction to the design of key RF building blocks used in high data rate transmitters emphasizes CMOS circuit techniques applicable to oscillators and upconvertors. The book is written in an easily accessible manner, without losing detail on the technical side.

CMOS RF Modeling, Characterization and Applications

This book, first published in 2004, is an expanded and revised edition of Tom Lee's acclaimed RFIC text.

Analysis and Design of RF CMOS Attenuators

VLSI-SoC: Forward-Looking Trends in IC and Systems Design

This book is written for academic and professional researchers designing communication systems for pervasive and low power applications. There is an introduction to wireless sensor networks, but the main emphasis of the book is on design techniques for low power, highly integrated transceivers. Instead of presenting a single design perspective, this book presents the design philosophies from three diverse research groups, providing three completely different strategies for achieving similar goals. By presenting diverse perspectives, this book prepares the reader for the countless design decisions they will be making in their own designs.

High Data Rate Transmitter Circuits

Electrical Overstress (EOS) continues to impact semiconductor manufacturing, semiconductor components and systems as technologies scale from micro- to nano-electronics. This bookteaches the fundamentals of electrical overstress and how to minimize and mitigate EOS failures. The text provides a clear picture of EOS phenomena, EOS origins, EOS sources, EOS physics, EOS failure mechanisms, and EOS on-chip and system design. It provides an illuminating insight into the sources of EOS in manufacturing, integration of on-chip, and system level EOS protection networks, followed by examples in specific technologies, circuits, and chips. The book is unique in covering the EOS manufacturing issues from on-chip design and electronic design automation to factory-level EOS program management in today’s modern world. Look inside for extensive coverage on: Fundamentals of electrical overstress, from EOS physics, EOS time scales, safe operating area (SOA), to physical models for EOS phenomena EOS sources in today’s semiconductor manufacturing environment, and EOS program management, handling and EOS auditing processing to avoid EOS failures EOS failures in both semiconductor devices, circuits and system Discussion of how to distinguish between EOS events, and electrostatic discharge (ESD) events (e.g. such as human body model (HBM),

charged device model (CDM), cable discharge events (CDM), charged board events (CBE), to system level IEC 61000-4-2 test events) EOS protection on-chip design practices and how they differ from ESD protection networks and solutions Discussion of EOS system level concerns in printed circuit boards (PCB), and manufacturing equipment Examples of EOS issues in state-of-the-art digital, analog and power technologies including CMOS, LDMOS, and BCD EOS design rule checking (DRC), LVS, and ERC electronic design automation (EDA) and how it is distinct from ESD EDA systems EOS testing and qualification techniques, and Practical off-chip ESD protection and system level solutions to provide more robust systems Electrical Overstress (EOS): Devices, Circuits and Systems is a continuation of the author's series of books on ESD protection. It is an essential reference and a useful insight into the issues that confront modern technology as we enter the nano-electronic era.

Proceedings of the ACM Great Lakes Symposium on VLSI.

With the growth of high-speed telecommunications and wireless technology, it is becoming increasingly important for engineers to understand radio frequency (RF) applications and their sensitivity to electrostatic discharge (ESD) phenomena. This enables the development of ESD design methods for RF technology, leading to increased protection against electrical overstress (EOS) and ESD. ESD: RF Technology and Circuits: Presents methods for co-synthesizisng ESD networks for RF applications to achieve improved performance and ESD protection of semiconductor chips; discusses RF ESD design methods of capacitance load transformation, matching network co-synthesis, capacitance shunts, inductive shunts, impedance isolation, load cancellation methods, distributed loads, emitter degeneration, buffering and ballasting; examines ESD protection and design of active and passive elements in RF complementary metal-oxide-semiconductor (CMOS), RF laterally-diffused metal oxide semiconductor (LDMOS), RF BiCMOS Silicon Germanium (SiGe), RF BiCMOS Silicon Germanium Carbon (SiGeC), and Gallim Arsenide technology; gives information on RF ESD testing methodologies, RF degradation effects, and failure mechanisms for devices, circuits and systems; highlights RF ESD mixed-signal design integration of digital, analog and RF circuitry; sets out examples of RF ESD design computer aided design methodologies; covers state-of-the-art RF ESD input circuits, as well as voltage-triggered to RC-triggered ESD power clamps networks in RF technologies, as well as off-chip protection concepts. Following the authors series of books on ESD, this book will be a thorough overview of ESD in RF technology for RF semiconductor chip and ESD engineers. Device and circuit engineers working in the RF domain, and quality, reliability and failure analysis engineers will also find it a valuable reference in the rapidly growing are of RF ESD design. In addition, it will appeal to graduate students in RF microwave technology and RF circuit design.

Wireless Radio-Frequency Standards and System Design: Advanced Techniques

CMOS technology has now reached a state of evolution, in terms of both frequency and noise, where it is becoming a serious contender for radio frequency (RF) applications in the GHz range. Cutoff frequencies of about 50 GHz have been

reported for 0.18 æm CMOS technology, and are expected to reach about 100 GHz when the feature size shrinks to 100 nm within a few years. This translates into CMOS circuit operating frequencies well into the GHz range, which covers the frequency range of many of today's popular wireless products, such as cell phones, GPS (Global Positioning System) and Bluetooth. Of course, the great interest in RF CMOS comes from the obvious advantages of CMOS technology in terms of production cost, high-level integration, and the ability to combine digital, analog and RF circuits on the same chip. This book discusses many of the challenges facing the CMOS RF circuit designer in terms of device modeling and characterization, which are crucial issues in circuit simulation and design.

Nano-scale CMOS Analog Circuits

The Design of CMOS Radio-Frequency Integrated Circuits

This book contains extended and revised versions of the best papers presented at the 18th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2010, held in Madrid, Spain, in September 2010. The 14 papers included in the book were carefully reviewed and selected from the 52 full papers presented at the conference. The papers cover a wide variety of excellence in VLSI technology and advanced research. They address the current trend toward increasing chip integration and technology process advancements bringing about stimulating new challenges both at the physical and system-design levels, as well as in the test of theses systems.

Asia Electronics Industry

This modern, pedagogic textbook from leading author Behzad Razavi provides a comprehensive and rigorous introduction to CMOS PLL design, featuring intuitive presentation of theoretical concepts, extensive circuit simulations, over 200 worked examples, and 250 end-of-chapter problems. The perfect text for senior undergraduate and graduate students.

The gm/ID Methodology, a sizing tool for low-voltage analog CMOS Circuits

Bridges the gap between device modelling and analog circuit design. Includes dedicated software enabling actual circuit design. Covers the three significant models: BSIM3, Model 9 &, and EKV. Presents practical guidance on device development and circuit implementation. The authors offer a combination of extensive academic and industrial experience.

Ultra-Low Power Wireless Technologies for Sensor Networks

This book provides the most comprehensive and in-depth coverage of the latest circuit design developments in RF CMOS technology. It is a practical and cutting-edge guide, packed with proven circuit techniques and innovative design methodologies for solving challenging problems associated with RF integrated

circuits and systems. This invaluable resource features a collection of the finest design practices that may soon drive the system-on-chip revolution. Using this book's state-of-the-art design techniques, one can apply existing technologies in novel ways and to create new circuit designs for the future.

Design of CMOS Phase-Locked Loops

In the world of optical data communications this book will be an absolute must-read. It focuses on optical communications for short and very short distance applications and discusses the monolithic integration of optical receivers with processing elements in standard CMOS technologies. What’s more, it provides the reader with the necessary background knowledge to fully understand the trade-offs in short-distance communication receiver design and presents the key issues to be addressed in the development of such receivers in CMOS technologies. Moreover, novel design approaches are presented.

ROMANCE ACTION & ADVENTURE MYSTERY & THRILLER BIOGRAPHIES & HISTORY CHILDREN'S YOUNG ADULT FANTASY HISTORICAL FICTION HORROR LITERARY FICTION NON-FICTION SCIENCE FICTION